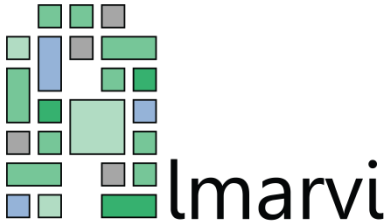

ALMARVI

"Algorithms, Design Methods, and Many-Core Execution Platform for Low-Power Massive Data-Rate Video and Image Processing"

Project co-funded by the ARTEMIS Joint Undertaking under the

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D7.9 - Standardisation efforts

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V0.1	17/10/2016	template	Draft	Almarvi
V0.2	11/01/2017	Added pocl and TCE open source release discussion. Removed Khronos and HSA as there was no contribution from ALMARVI side.	Draft	Almarvi
V0.033	30/01/2017	TUDelft contribution to MCA and OPF sections Added SDF3, TRACE and OctoSim and removed Poosl	Draft	Almarvi
V0.4	20/02/2017	removed DICOM and HL7 as they are related to healthcare interfaces and not related to Almarvi topics	Draft	Almarvi
V0.5	17/03/2017	Added introduction, summary and conclusions	Draft	Almarvi
V1.0	30/03/2017	Approved for submission to ARTEMIS JU	Final	Artemis

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Glossary

Abbreviation / acronym	Description
HSA	Heterogeneous Systems Architecture.
MCA	Multi-core Association
pocl	Portable Computing Language, an open source implementation of the Khronos OpenCL standard.
SDF3	Synchronous Data Flow For Free
TRACE	Tool for visualization and analysis of execution traces
TCE	TTA-Based Co-Design Environment
ρVEX	Reconfigurable VLIW example

1. Introduction

The Almarvi project, deals with performance and power use of image processing systems. The innovative aspect is to ensure high performance and low power usage for multi-core image processing applications, through a 3-layered architecture, separating the applications from the system layer with run-time support dealing with performance and power issues. The most important standards identified for the project deal with multi-core development (MCA) and with low power use (OpenPOWER foundation).

In the diverse application domains standards bodies deal with the quality and interfaces for devices. As the project is concentrating on cross-domain image processing improvements, such domain-specific standard are not relevant. However for certain aspects in the project open source initiatives are relevant. Such open source initiatives produce de-facto standard solutions for a problem that is relevant for the community. For the Almarvi project the following open source initiatives are relevant, as their solutions are in use for the Almarvi results or demonstrators. The most important open source initiatives are pocl, TCE, ρVEX, OctoSim, SDF3, TRACE.

For each of the standard bodies, ch. 2, and open source initiatives, ch. 3, it is explained relevant changes during the Almarvi project time, influence on the Almarvi project and/or vice versa. For the open source initiatives an outlook of future relevant development is presented.

2. Important Funding bodies

2.1 Multi-core association (MCA)

The Multicore Association (MCA) is a non-profit organization that focuses on addressing the challenges of creating portable multicore system solutions across the industry. MCA tackles the issues of multitasking and communication APIs and debug. Its goal is to provide a forum in which all relevant multicore standardization issues can be discussed and resolved. Ultimately, the objective is to give members the ability to certify their products according to MCA standards.

2.1.1 Relevant discussions in MCA between 2014 and 2017

In the past 3 years, MCA has been developing a number of industry multicore standards. Relevant discussions to ALMARVI can be represented by 3 different workgroups in MCA: MCAPI, SHIM and OpenAMP.

1. The Multicore Communications API (MCAPI) specification defines an API and a semantic for communication and synchronization between processing cores in embedded systems.
2. The SHIM Working Group is the Software-Hardware Interface for Multi-Many Core. It provides a common interface to abstract the hardware properties that matter to multicore tools.
3. The Open Asymmetric Multi Processing Framework (OpenAMP) working group provides an open source framework that allows operating systems to interact within a broad range of complex homogeneous and heterogeneous architectures and allows asymmetric multiprocessing applications to leverage parallelism offered by the multicore configuration.

2.1.2 Influence of MCA standards on Almarvi results

ALMARVI partners evaluated the effectiveness of MCA MCAPI specification as an alternative interface for abstracting heterogeneous hardware architectures. This evaluation is discussed in the ALMARVI deliverable D3.3. It was noted that MCAPI is the prevalent industry-standard API for light-weight heterogeneous distributed-memory systems, as maintained by the multi-core association (MCA). More specifically, MCAPI provides light-weight channel constructs to communicate messages between heterogeneous components.

However, the ALMARVI partners chose for the more open standard and more widely supported OpenCL specification for the project.

2.2 OpenPower foundation (OPF)

The OpenPOWER Foundation (OPF) was founded in 2013 as an open technical membership organization that will enable members to rethink their approach to the processing technology. Member companies are enabled to customize POWER CPU processors and system platforms for optimization and innovation for their business needs. These innovations include custom systems for compute intensive applications, workload acceleration through GPU, FPGA or advanced I/O, platform optimization for SW appliances, or advanced hardware technology exploitation.

2.2.1 Relevant discussions in OpenPower foundation between 2014 and 2017

The OPF has a number of workgroups with various activities that is related to computer architecture and high-throughput image processing. One of the most relevant workgroups to the ALMARVI project is the Accelerator workgroup. This workgroup defines, documents, manages, and maintains standards, which define the interfaces between the processor and accelerator devices and their associated development tools. This includes hardware, firmware and any other software required for accelerators to operate within OpenPOWER compliant systems. It will also identify future requirements and propose innovations to the interfaces to enable advances in accelerator capabilities and work with other working groups as appropriate.

2.2.2 Standardisation in OpenPower foundation of Almarvi results

The OPF accelerator workgroup has been working on defining standardized interfaces that enable applications to access hardware accelerators transparently. Part of the innovation is originating from the shared memory interface that OPF systems used to access the host as well as the accelerator memory using a unified address space on the computer system. Another part of the innovation is in defining standardized methods to call accelerators irrespectively of the specific application or hardware platform used.

The TUDelft lead the definition and implementation of the SNAP interface that OPF announced in November 2016. This interface makes it easy for any application programmer to use existing accelerator resource on the system by calling it using a unified interfacing API. The development of this interface was facilitated and influenced by the effort and experiences that the TUDelft gained during the work within the ALMARVI project.

3. Open source initiatives

3.1 pocl

pocl stands for Portable Computing Language. It is an open source implementation of the Khronos OpenCL standard that was used and extended in ALMARVI project.

3.1.1 Development of pocl between 2014 and 2017

ALMARVI project provided basis for supporting FPGA IP blocks from the pocl's OpenCL framework. The first prototype of the integration interface, AlmaIF was successfully supported by the pocl's driver framework. In this use, pocl provided the basis for the "ALMARVI software stack" and on the other hand, provided useful feedback to pocl side for supporting FPGA integration.

During the ALMARVI work, several features such as proper support for offline compilation of kernels for embedded systems without online compiler support was added to pocl framework. In addition, task level parallelization of multiple kernel applications was implemented and contributed to open source. Multiple open source releases of pocl were managed with the sponsorship from the ALMARVI project.

3.1.2 Outlook

It is envisioned that the FPGA IP support will be continued in the future projects with the aim of going towards the HSA standard in its interface. ALMARVI project and its hardware platform provided excellent ground to study problems in rapid FPGA integration of custom hardware blocks such as the application specific processors produced with the TCE toolset and the runtime reconfigurable VLIWs from TUDelft. On this basis it should be much easier to build a more efficient version of the FPGA support which exploits on chip streaming to the maximum and is user friendly enough for a wider audience.

3.2 TCE

TTA-Based Co-Design Environment (TCE) was used for designing several custom processor cores within the ALMARVI project.

3.2.1 Development of TCE between 2014 and 2017

TCE toolset was extended within ALMARVI with various features required to support the novel features in the developed demonstrator designs. Large part of the effort was spent on the compiler side due to the static nature of the processor architecture. Also various usability features were added thanks to the feedback gathered during the design experiments conducted in the project. The most visible effect to the TCE source code of ALMARVI was the specification of AlmaIF v1 integration interface. Features required to generate automatically AlmaIF v1 compatible TCE cores are now integrated to the open source TCE which makes it very easy to plug in TCE based designs to system architectures. Also, all in all, the open source version of TCE was maintained with multiple releases made within the project span which would not have been possible without the ALMARVI funding.

3.2.2 Outlook

Development of TCE open source project is expected to go on in the future projects with new features developed in ALMARVI accelerating its adoption both in academic and commercial setting.

3.3 ρVEX

The ρVEX dynamically reconfigurable VLIW processor project has a long history of releasing code and other resources into the public domain, starting with the first version in 2008. At this time, there are HDL designs, tools and teaching materials available for download from the project website under an academic license.

3.3.1 Relevant discussions in ρVEX between 2014 and 2017

During the ALMARVI project, a ρVEX website has been set up at http://rVEX.ewi.tudelft.nl to host releases relevant to other researchers and teachers. The ρVEX is now aiming to be not only a proof-of-concept of a dynamic VLIW processor, but also a platform that other labs can use as a basis for research on VLIWs. The maturity of the tools and designs have improved considerably during the ALMARVI project, making the codebase suitable for this purpose.

In addition to this development, a new research branch has been started using the ρVEX platform, aiming to develop an FPGA overlay fabric targeting streaming image processing applications. Initial work in this direction has been accepted for publication and the intention is to release the code on the project website.

Regarding standardization, the ρVEX internal busses have been connected to the AXI standard used for the ALMARVI prototypes and an interface has been implemented in accordance with the ALMARVI specifications. Combined with the LLVM back-end implemented in 2015, this allows the ρVEX to be used as a compute unit in the POCL OpenCL framework.

3.3.2 Outlook

Final efforts are being made to release the newest version of all designs and tools in an integrated release package that includes simulation, synthesis, compilation and testing frameworks to facilitate rapid simulation and prototyping on FPGA boards. It is expected to be released shortly. Additionally, an effort has been started in cooperation with one of TUDelft's Microelectronics research groups, to tape-out an ASIC implementation of the processor in Q3 2017. This effort aims to show the viability of the dynamic concepts and allow us to do power evaluations.

3.4 OctoSim

OctoSim is an embedded domain-specific language that can be used to create and simulate abstract models of parallel sets of tasks with data dependencies that share resources (Hendriks et al. 2016). The tool has been used in the Almarvi project for modelling and analysis of a part of the Philips Healthcare case study.

3.4.1 Outlook

No future developments of OctoSim are anticipated.

3.5 SDF3

SDF3 [1] (Synchronous Data Flow For Free) is an open source tool that supports, among other things, the analysis of dynamic dataflow models and a design-flow to map dataflow applications to predictable multiprocessor platforms. It has been developed by the TUE. It has been used and extended in the Almarvi project.

3.5.1 Relevant development in SDF3 between 2014 and 2017

During the Almarvi project period, the SDF3 tool has extended its analysis capabilities. The following extensions have been made through the Almarvi project.

- Techniques have been implement to efficiently generate execution traces for so-called FSM-SADF dynamic dataflow models. The output can be connected to the Trace visualisation tool used in Almarvi; see section 3.6.
- Analysis techniques for improved efficiency of asynchronous distributed shared resource arbitration have been implemented.

Efficient analysis of throughput and latency of multi-scale data processing applications, such as image processing application are currently being implemented.

3.5.2 Outlook

Anticipated future developments for SDF3 include:

- Analysis and synthesis algorithms will be further strengthened.
- Use and interpretation of results will be facilitated with connections to domain specific languages, models and visualisations.
- Core algorithmic solutions for max-plus algebra computations and graph / game-theoretic algorithms will be exposed as separate libraries for use by a broader community than dataflow and multiprocessor systems.

3.6 TRACE

TRACE (http://trace.esi.nl/) is a domain-independent tool for visualization and analysis of execution traces – time-stamped sequences of start- and end-events of activities. Execution traces can be generated from models, by a wide variety of modelling and analysis tools, and from prototypes, through instrumentation of software.

3.6.1 Relevant development in TRACE between 2014 and 2017

During the Almarvi project period, the TRACE tool has extended its analysis capabilities. The following extensions have been made through the Almarvi project:

- Critical path analysis
- Distance analysis
- Resource-usage analysis
- Metric Temporal Logic (MTL) checking

3.6.2 Outlook

Anticipated further developments for TRACE include a domain-specific language to specify often-used timing properties such as latency and throughput. This builds upon the MTL framework and eases the use of this formal specification and analysis mechanism.

4. Executive Summary

This document describes the relevant standards and open source initiatives for the Almarvi project. The most important standards are the MCA for multi-core development and the OpenPOWER foundation for low power use. The document also describes six relevant open source initiatives that provide (de-facto) standards relevant for the Almarvi topics: image processing on multi-core with low power usage.

Activities in MCA involved several interfaces needed for multi-core image processing. Influence on Almarvi is limited as the project adopted the widely supported OpenCL tool support. Several Almarvi results are adopted for standardisation by the OpenPOWER foundation.

For open source initiatives:

- the pocl development was important as it provides basic building blocks for the Almarvi software stack;
- Involvement of Almarvi in TCE led to the specification of the AlmaIF v1 integration interface;
- The ρVEX development was an important element in the use of FPGA boards for image processing for several project partners;
- The OctoSIM tool was useful in modelling and analysis of resource use of applications;
- SDF3 was improved with Almarvi-relevant extension on execution traces and analysis of efficiency;
- The TRACE tool for visualising traces developed several extensions that were relevant for Almarvi

These standardisation and open source improvements help to sustain the Almarvi results after project end.

5. References

[1] S. Stuijk, A. Basten and M. Geilen, “SDF3: SDF For Free,” in *Application of Concurrency to System Design, 6th International Conference, ACSD 2006, Proceedings*, 2006.